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Dual AGC model based implementation of Auditory Nerve

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ABSTRACT

Conventional automatic speech recognizer doesn't perform well within the presence of noise. In this paper a unique feature based on associate auditory nerve model for strong speech recognition is proposed. Auditory nerve circuit using a dual AGC (Automatic Gain Control) model has been implemented using 180nm technology. This model needs a dramatic rethinking of the way to method sound signals. This approach is named biomimetic that is mimicking nature's biological systems. For these auditory systems, portions of the mammalian cochlea are often implemented using analog very large scale integration (VLSI). This shows applicable circuits will have the importance of accuracy mismatch signal using analog VLSI and can be used with only of average power.

KEY WORDS: Auditory nerve, biomimetic, very large scale integration (VLSI), dual AGC.

1. INTRODUCTION

This work focus on the analog VLSI implementation of auditory models using current mode techniques. It can be used for sound source localization. The goal is to develop a successful path to implement such structures in respect to manufacturability. The auditory model is a parallel system of non-linear function that is implemented in analog circuitry, the main challenge is to find an implementation that can accommodate mismatch and process deviation under given design constrains such as chip area and power. For these auditory systems, portions of the mammalian cochlea are often implemented using analog very large scale integration (VLSI). In these implementations can typically be divided into three stages before reaching the higher level audio functions. These stages are: frequency selectivity, which mimics the basilar membrane; adaptation or automatic-gain-control (AGC), which increases the dynamic range and accentuates signal onsets; and one-bit spiking neuron digitization, as the auditory nerve action potential is often represented in neuromorphic processors.

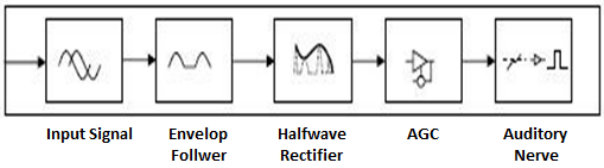

Figure.1.Processing stage of the auditory nerve model

The output of the auditory nerve (AN) is defined as an instantaneous spike rate (ISR) shown in Fig1. The ISR outputs are representative of providing a sound repeatedly and measuring the spiking events within a short duration. This is called a post-stimulus time histogram (PSTH) and is equivalent to looking at many nerve fibers simultaneously for just one presentation of a sound.

2. METHODOLOGY

The dual AGC current-domain circuit Fig 2 begins with an envelope follower that consists of a half-wave rectifier (HWR) that is buffered with a fully-balanced current mirror (FBCM). The buffered signal feeds two stages of low-pass filtering. Adaptation is performed in the dual AGC stage where both pre- and post-synaptic effects are replicated. Fully-balanced current mirrors (FBCM) provide impedance matching for the multiplier (MULT) and low-pass filter (LPF) circuits. Subtraction (SUB) circuits in the AGC provide a reference current level, K1 or K2, from which the filtered feedback signal is compared.

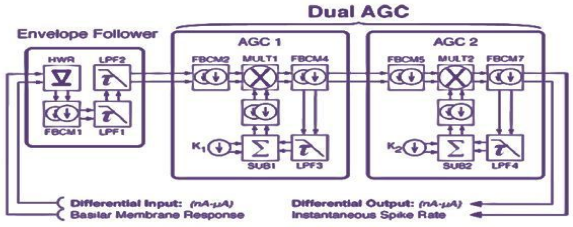

Figure.2.Block diagram

Dual AGC model: AGCs are engineered by having a variable gain electronic equipment (VGA). It varies its gain specified soft sounds that are amplified with an oversized gain whereas loud sounds are amplified weak or maybe attenuated. If the intensity of the incoming sound changes without giving the notice, then an AGC can take time to adapt to the new sound level and change its gain. Widely used AGCs in bionic ear processors have one attack time constant for soft-to-loud transitions and one unharness time constant for loud-to-smooth transitions and represent a single-loop AGC. The attack time constant is invariably faster than the discharge time constant. Dual-loop ways have

two sets of attack and unharness time constants, a slow set and a quick set. The slow set adapts comparatively slow to the general sound level, increasing listening comfort within the surroundings, and is usually in use.

Auditory nerve integrated circuit (ANIC) in a current mode implementation: Current mode technology allows the implementation of certain signal processing stages in a very elegant and simple fashion. A good example is the current mirror that allows addition and subtraction, as well as the multiplication. Another advantage is the adjustment of dynamic range by varying the bias current accordingly. In the case of a low impedance implementation, a high dynamic range can be achieved without increasing the power supply voltage. Current mode techniques are also well known in the RF community and are well established in low voltage differential signaling communication channels. In this work, the choice of implementation is continuous time current mode circuitry.

The dual AGC model has been enforced on a spread of electronic platforms together with code simulations, discrete analog natural philosophy DSPs victimization, Analog Device's FPGAs and digital ASICs. The current power envelopes of those platforms limit their usage in mobile applications. wherever acoustic sensors will have the foremost impact to beat this power constraint, associate analog VLSI cranial nerve circuit, referred to as the AN circuit, is enforced victimization current-mode CMOS circuits.

The dual AGC model is reworked into this domain as shown in Fig. 3, with the model constants and having analogous terms within the current domain. The time constants are brought directly from the twin AGC model rather than counting on the copious amounts of gain that voltage-mode circuit offer. We have a tendency to believe the matching of CMOS current-mode circuits to implement low-power natural philosophy with ample dynamic variation despite today's low offer voltage technology. It ought to be expressed that almost all current-mode circuits use weak inversion MOSFETs in log-domain filters to attain giant dynamic ranges and to perform trans linear multiplication exactly due to the poor matching properties of weak inversion MOSFET's that cannot be overcome with remunerated layout techniques like common-centroid layouts. Its usage was unbroken to a minimum by solely victimization weak inversion MOSFETs within the low-pass filter's operational trans conductance electronic equipment (OTA). By concentration on current-mode CMOS circuits that aren't in operation in weak inversion, we have a tendency to primarily concern ourselves with the non-ideal current mirroring of CMOS transistors. This has the helpful effect of permitting differential-mode circuit topology thus we can consider the upper degree of current mirroring as compared to weak inversion MOSFETs. We can able to reject unwanted common-mode signals associated with the circuits by using a totally differential current-mode design.

Auditory Nerve IC Circuits:

Fully balanced current mirror: A fully balanced current mirror allows differential current type of operation with good common mode rejection ratio. The circuit implementation consists of two sources M3 and M10 that are biased with current source matching the bias current of Iref. These current source were removed and the differential signal path was closed by replaced with current mirror following the signal current within the branch M4 and M11. This will reduce the biasing circuit complexity. Further the CMRR is enhanced using the voltage sources M3 and M10.

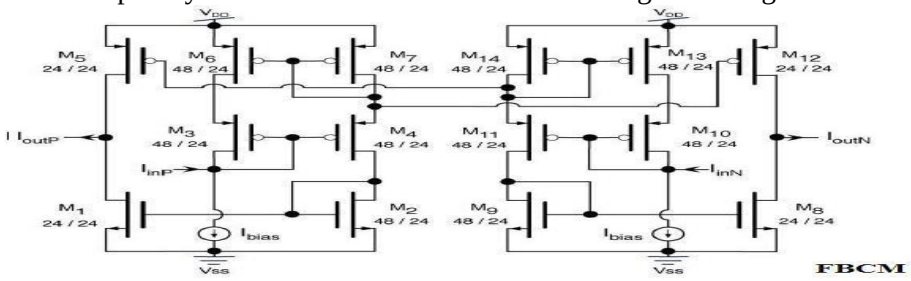

Figure.3.Fully balanced current mirror

Rectifier: Full and half-wave rectifiers are important building blocks for analog signal processing. The most common application for a full-wave rectifier is it's usage in automatic gain control loops. Fig.4 shows the RMS detectors and peak detectors. In conjunction with high performance Op amps and diodes, very precise rectifiers can be realized.

Current-Mode Low Pass Filter: The circuit for a current-mode low pass filter is shown in Fig.5.

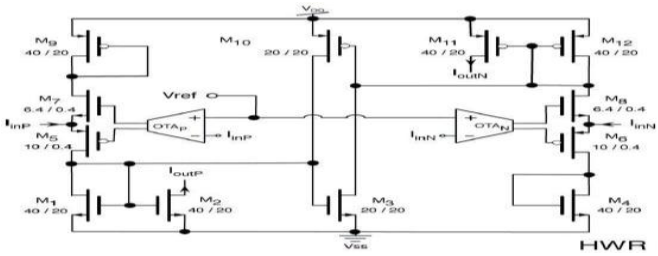

Figure.4.Half wave rectifier

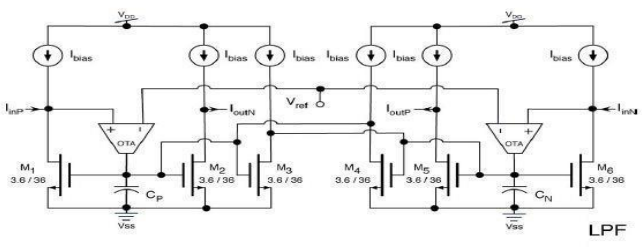

Figure.5.Low pass filter

The low pass filter is used to filter the high frequency signal. Based on the architecture of this design, general improvements to the filter structure were conducted. The design goal was to improve tuning range, dynamic range and power consumption. From an operating stand-point, the main difference between the two filters is the mode of operation. The original design operated the active devices for the filter operation in saturation, whereas this design operates purely in the Mode region. This mode of operation allows using the internal reference voltage V as a tuning parameter for the cut-off frequency by controlling the trans conductance of the active devices. In the original design, the cut-off frequency is controlled by Vo, of the internal trans conductance of the operational trans conductance amplifier (OTA). The second tuning parameter will allows in combination with Vo, a filter operation down to 1 Hz. Hence, a tuning range of 1 Hz to 1 kHz can be achieved, which is within the requirements of the auditory nerve models.

Current Mode Multiplier: Analog multipliers are important elements for analog signal processing systems. Multipliers find usage in linear amplitude modulators, AGC amplifiers, variable quadrature oscillators and variable gain amplifiers. The squaring feature of a multiplier gives also access to frequency doubling and full wave rectification. In general, multipliers are typically better described as current mode rather than voltage mode. In voltage mode circuits, a voltage is converter to a current that is biased in saturation, the current is proportional to the square law. Squaring techniques allow the manipulation of the input signals in such a way that a multiplication results in the current domain. The signal is converted back to a voltage signal. In current mode multipliers, the signal processing path stays in the current domain. If the input signal is current, the manipulation is performed in the current domain, and the output is again a current. Most MOS multipliers have in common is, they exploit the square law dependency of the drain current on the gate voltage. The only exceptions are circuits using the trans linear principle. Here transistors are biased in sub-threshold to achieve an exponential dependence and this is of course true for the original implementation, using transistor. The trans linear principle is based on the linear dependence.

Operational Trans conductance Amplifier: Operational trans conductance amplifier shown in Fig.6 is used as a level shifter and it keeps the transistor biased. Design of operational trans conductance amplifier is done and it is used for the above circuits like half wave rectifier and low-pass filter.

Envelop follower: The envelop follower consist of three circuits such as HWR, FBCM and LPF. The detailed block diagram is shown in Fig.2. Each circuit checks individually and integrate all the blocks.

Simulation results: The simulation results obtained using LT spice software for a fully balanced current mirror is shown in Fig.5. This will act as a buffer circuit. The OTA circuit design is shown in Fig.6 and the obtained level shifted waveform is shown in Fig.7. OTA amplifies the differential input voltage and gives the amplified output. Here OTA is used for converting voltage to current. Fig.8 shows the half wave rectifier positive side wave form. Fig.9 indicates the low pass filter output and response of emitter follower is shown in Fig.10. The simulation output for the designed AGC circuit is shown in Fig.11.

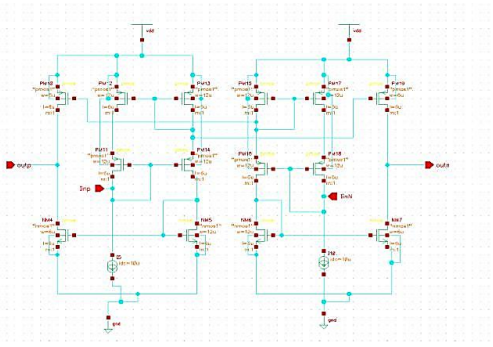

Figure.6.Fully balanced current mirror

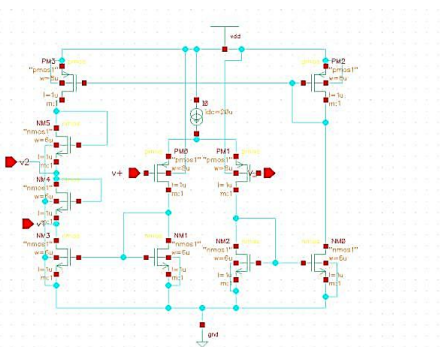

Figure.7.OTA circuit

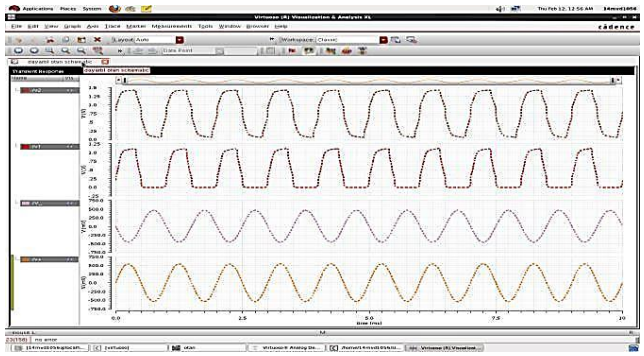

Figure.8.OTA results

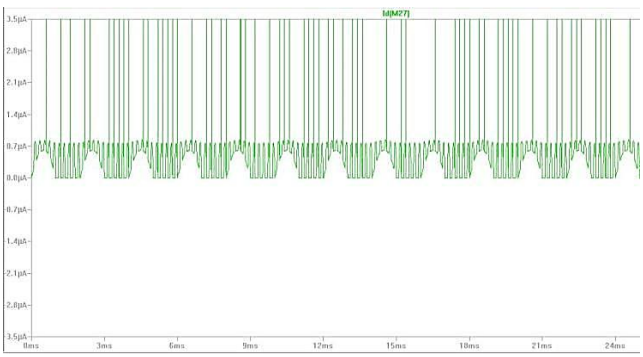

Figure.9.Half wave rectifier positive side wave form

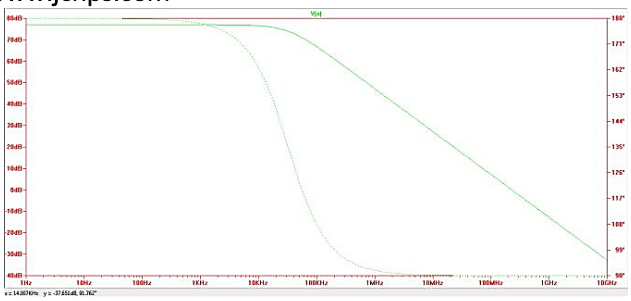

Figure.10.Low pass filter

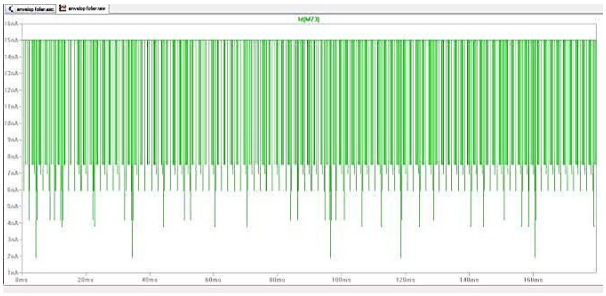

Figure.11.Envelop follower

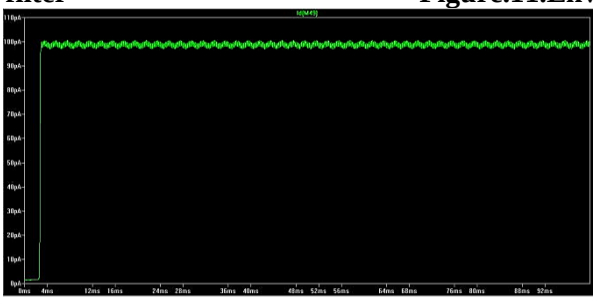

Figure.12.Dual AGC

The table shows the current consumption, number of occurrence and the current consumption in each block of AGC circuit. Thus the overall average power consumption for dual AGC is 3.2mW. This average power consumption very lesser than the conventional speech recognizer because it takes power 100mw. The change from low to high frequency is obtained with variation of less average power.

Table.1.Current consumption of each block

Blocks	Current consumption	Occurrence	Current consumption
HWR	< 1U	1	< 1U
FBCM	60 U	6	360 U
LPF	70 U	4	280 U
MULT	200 U	2	400 U
AGC	390 U	2	780 U
DUAL AGC			1820 U

3. CONCLUSION

An analog VLSI implementation of the dual AGC model for use in monaural, binaural, or multiple binaural systems has been presented. The dual AGC model has been transformed into the current domain using differential current-mode circuits and can be used with only of average power. This removal allows faithful reproduction of the dual AGC circuit over a large batch of fabricated devices. This results have been evaluated using tests established by Meddis mode. The low-power envelope, real-time processing, and behavior flexibility from various levels of tenability make the AN IC a practical module for use in biomimetic processing, especially in mobile and battery powered applications where the AN IC can be easily integrated into existing and future systems.

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